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1. (Currently Amended) A method for fabricating an NAND type non-volatile ferroelectric memory cell, comprising the steps of:

(1) forming an N number of wordlines and a WEC electrode on a first conduction type semiconductor substrate at fixed intervals;

(2) forming ferroelectric capacitor first electrodes over the wordlines excluding ~~an (N)th wordline~~ the WEC electrode with a barrier metal disposed in-between;

(3) forming a capacitor electrode material on the WEC electrode;

~~(3)~~(4) forming ~~source and drain~~ impurity regions in the substrate on both sides of the ferroelectric capacitor first electrodes and the WEC electrode;

~~(4)~~(5) forming a ferroelectric film at sides and top of the ferroelectric capacitor first electrodes and the capacitor electrode material;

~~(5)~~(6) forming ferroelectric capacitor second electrodes on the ferroelectric film;

(7) deposing an insulating film on entire structure after removing the ferroelectric film and the ferroelectric capacitor second electrode formed on the WEC electrode;

(8) forming contact holes to expose the impurity regions excluding first and last impurity regions and to expose a portion of each ferroelectric capacitor second electrode;

~~(6)~~(9) forming plugs for connecting each impurity region to the ferroelectric capacitor second electrode, respectively; ~~the source and drain regions to the ferroelectric capacitor second electrodes adjacent to the source and drain regions respectively excluding the first region and the (N)th region of the N numbers of the source and drain regions; and,~~

(10) depositing the insulating film after forming the plugs;

(11) forming contact holes to expose the first and the last impurity regions; and

(12) filling conductive material with the contact holes for the first and the last impurity regions; and

(13) thereby forming bitlines

~~(7) bitlines formed on the substrate inclusive of the plugs with an insulating layer disposed inbetween for electrically connection to the first region and (N)th region of N number of the source and drain regions.~~

2. (Original) A method as claimed in claim 1, wherein the steps (1) and (2) includes the steps of;

(10-1) forming a gate insulating film on a first conduction type semiconductor substrate;

(10-2) forming a wordline material layer on the gate insulating film;

(10-3) forming a barrier metal layer on the wordline material layer;

(10-4) forming a capacitor electrode material layer on the barrier metal layer; and

(10-5) selectively removing the capacitor material layer, the barrier metal layer, the wordline material layer, and the gate insulating film, to form wordlines insulated from the substrate by the gate insulating film, and first electrodes with the barrier metal layer disposed between the first electrodes and the wordlines.

3. (Original) A method as claimed in claim 2, further comprising the step of stuffing a space between every adjacent wordlines with an insulating material until sides of the barrier metal layer are exposed after the step (10-5).

CLAIMS 4-9. (CANCELLED)

10. (New) A method for fabricating an NAND type non-volatile ferroelectric memory cell, comprising the steps of:

(1) forming an N number of wordlines on a first conduction type semiconductor substrate at fixed intervals;

(2) forming ferroelectric capacitor first electrodes over the wordlines excluding an (N)th wordline with a barrier metal disposed inbetween, wherein the ferroelectric capacitor first electrodes are electrically connected to the wordlines formed underneath through the barrier metal;

(3) forming combined source and drain regions in the substrate on both sides of the ferroelectric capacitor first electrodes;

(4) forming a ferroelectric film at sides and top of the ferroelectric capacitor first electrodes;

(5) forming ferroelectric capacitor second electrodes on the ferroelectric film;

(6) forming plugs for connecting the combined source and drain regions to the ferroelectric capacitor second electrodes adjacent to the source and drain regions respectively excluding the first region and the (N)th region of the N numbers of the combined source and drain regions; and

(7) bitlines formed on the substrate inclusive of the plugs with an insulating layer disposed inbetween for electrically connection to the first region and (N)th region of N number of the combined source and drain regions.